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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/673,324

09/30/2003

Yung-Hui Yeh

YEHY 3001 / EM

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06/07/2006

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EXAMINER

SANTIAGO, MARICELI

ART UNIT

PAPER NUMBER

2879

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/673,324	Applicant(s) YEH ET AL.	
	Examiner Mariceli Santiago	Art Unit 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The Amendment, filed on March 13, 2006, has been entered and acknowledged by the Examiner.

Cancellation of claim 2 has been entered.

Claims 1 and 3-12 are pending in the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 7-9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Eida (EP 1178709 A1).

Regarding claim 1, Eida discloses an active organic light emitting diode display structure (Fig. 17) comprises a glass substrate (10), an active component layer (44), disposed on the glass substrate, an intermediate insulate layer (12), disposed on the top of the active component layer (44), a color filter area (60), disposed on part of the surface of the intermediate insulate layer (60), an electrical conducting layer (228, 22), disposed above the color filter area (60), a black matrix layer (13, Page 15, Paragraph [0145]), disposed on the top surface of the electrical conducting layer (overlapping conductive member 28), and cover margins of the color filter area (60, overlapping margin of filter member 60), an organic light emitting diode layer (24), disposed on the black matrix layer (13), and a cathode layer (20), disposed in the organic light emitting diode layer (24).

Regarding claim 3, Eida discloses an active organic light emitting diode display structure wherein the active component layer is a buffer layer having poly-Si thin film transistors (poly-Si TFTs), (Page 9, paragraph 0068)).

Regarding claim 4, Eida discloses an active organic light emitting diode display structure wherein the color filter area (60) is coated on an area of the surface of the intermediate insulate layer (12).

Regarding claim 5, Eida discloses an active organic light emitting diode display structure wherein the electrical conducting layer is an indium tin oxide (ITO) layer (Page 12, paragraph [0111]).

Regarding claim 7, Eida discloses an active organic light emitting diode display structure wherein the black matrix layer is a black photo resist thin film (Pages 8-9, paragraphs [0053-0056]).

Regarding claim 8, Eida discloses an active organic light emitting diode display structure wherein the black matrix layer is disposed on the top surface of the electrical conducting layer, the black matrix layer has an opening, the opening is located above the color filter area, the area of the opening is lightly smaller than the area of the color filter area, and the black matrix layer covers margins of the color filter area as well as the non color filter area (Fig. 17). Eida states in Paragraph [0145] "It is also preferred to arrange, between the fluorescent medium pieces, a shading layer (black matrix) for blocking off the luminescence emitted from each organic EL element and the light incident from the respective fluorescent medium piece and for improving contrast so as to reduce the dependency upon the viewing angle". Accordingly, since the fluorescent medium pieces, located over the color filter area, are arranged in a pixel matrix array it is construed from Eida's teachings that the black matrix 13 surrounds the color filter area.

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Regarding claim 9, Eida discloses an active organic light emitting diode display structure wherein the organic light emitting diode is white organic light emitting diode (Page 14, paragraph [140]).

Regarding claim 11, the claims are directed to the method of manufacturing the electrical conducting layer by sputtering, in view of an absent of a showing that the method imparts distinctive structural characteristics to the final product, the limitations directed to the method of manufacturing are not germane to the issue of patentability of the device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eida (EP 1178709 A1).

Regarding claim 10, Eida discloses an active organic light emitting diode display structure wherein the black matrix layer is disposed on the top surface of the electrical conducting layer, the black matrix layer has an opening, the opening is located above the color filter area, the area of the opening is slightly smaller than the area of the color filter area, and the black matrix layer covers margins of the color filter area as well as the non color filter area (Fig. 17). Eida states in Paragraph [0145] "It is also preferred to arrange, between the fluorescent medium pieces, a shading layer (black matrix) for blocking off the luminescence emitted from each organic EL element and the light incident from the respective fluorescent medium piece and for improving contrast so as to reduce the dependency upon the viewing angle".

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Accordingly, since the fluorescent medium pieces, located over the color filter area, are arranged in a pixel matrix array it is construed from Eida's teachings that the black matrix 13 surrounds the color filter area. Eida fails to disclose the limitation of wherein the entirety of the black matrix layer is disposed on the top surface of the electrical conducting layer. At the time the invention was made, it would have been an obvious matter of design engineering to a person of ordinary skill in the art to provide the black matrix layer disposed in its entirety on the top surface of the electrical conducting layer since applicant's claimed location does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teaching applied. Furthermore, one skilled in the art would reasonable expect applicant's invention to perform equally well with either partially providing the black matrix layer over the top surface of the electrical conducting layer as disclosed by Eida or providing the black matrix layer in its entirety over the top surface of the electrical conducting layer as claimed since both arrangements perform the same function of blocking off the luminescence emitted from each organic EL element and the light incident from the respective fluorescent medium piece and for improving contrast so as to reduce the dependency upon the viewing angle. Accordingly, it would have been an obvious matter of design engineering to modify the device of Eida to obtain the invention as specified in claim 10.

Regarding claim 12, Eida discloses an active organic light emitting diode display structure (Fig. 17) wherein the active component layer is a buffer layer having poly-Si thin film transistors (poly-Si TFTs), (Page 9, paragraph 0068]), the color filter area (60) is coated on an area of the surface of the intermediate insulate layer (12), the electrical conducting layer (28) is an indium tin oxide (ITO) layer (Page 12, paragraph [0111]), the black matrix layer is a black photo resist thin film (Pages 8-9, paragraphs [0053-0056])., the organic light emitting diode is white organic light emitting diode (Page 14, paragraph [140]), the black matrix layer is disposed on the top surface of the electrical conducting layer, the black matrix layer has an opening, the

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opening is located above the color filter area, the area of the opening is lightly smaller than the area of the color filter area, and the black matrix layer covers margins of the color filter area as well as the non color filter area. Eida states in Paragraph [0145] "It is also preferred to arrange, between the fluorescent medium pieces, a shading layer (black matrix) for blocking off the luminescence emitted from each organic EL element and the light incident from the respective fluorescent medium piece and for improving contrast so as to reduce the dependency upon the viewing angle". Accordingly, since the fluorescent medium pieces, located over the color filter area, are arranged in a pixel matrix array it is construed from Eida's teachings that the black matrix 13 surrounds the color filter area.

In regards to the limitation "the entirety of the black matrix layer is disposed on the top surface of the electrical conducting layer" same rational stated in the rejection of claim 10 above applies.

In regards to the limitation "the electrical conducting layer is disposed on the intermediate insulate layer by sputtering", in view of an absent of a showing that the method imparts distinctive structural characteristics to the final product, the limitations directed to the method of manufacturing are not germane to the issue of patentability of the device.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eida (EP 1178709 A1) in view of Kadota et al. (US 5,818,550).

Regarding claim 6, Eida fails to exemplify the black matrix layer being a metal thin film. However, in the same field of endeavor, Kadota discloses the use of a metal thin film layer as a black matrix on the driving active region of the display (Column 7, lines 29-35). One skilled in the art would reasonably contemplate selection of a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was

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made to have the black matrix layer being a metal thin film, since the selection of known materials for a known purpose is within the skill of the art.

Response to Arguments


Applicant's arguments with respect to claims 1 and 3-12 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Mariceli Santiago
Primary Examiner
Art Unit 2879